Paper No. 17

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte ROSE A. MULLIGAN, JUN HE, THOMAS MARIEB, SUSANNE MENEZES and STEVEN TOWLE

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Appeal No. 2004-0999
Application 09/997,086

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ON BRIEF

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Before KRASS, FLEMING, and RUGGIERO, ***Administrative Patent Judges.***

FLEMING, ***Administrative Patent Judge***.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1-20. Claims 21-30 have been withdrawn.

INVENTION

Appellants' invention relates to the dicing of microelectronic device wafers into individual microelectronic dice, wherein trenches are formed in dicing streets of the microelectronic device wafer. These trenches assist in the

prevention of defects, such as, cracks and delamination, from forming and/or propagating in the interconnect layer of the integrated circuitry of the microelectronic device wafer. See Appellants' specification, page 1, lines 4-9. Appellants disclose at least one trench in the interconnect layer of a microelectronic device wafer such that at least one wall of each trench will be positioned on either side of where a wafer saw will cut through the microelectronic device wafer. See Appellants' specification, page 6, lines 1-3.

Appellants' Fig. 1 illustrates a microelectronic device wafer 100 similar to the prior art microelectronic device wafer 200 of Figs. 15 and 16 comprising a semiconductor wafer 114 mounted onto a sticky, flexible tape 116 and an interconnect layer 108 disposed on the semiconductor wafer 114. The interconnect layer 108 is generally alternating layers 112 of dielectric material and patterned electrically conductive material. See Appellants' specification, page 6, lines 4-15. A plurality of dicing streets 104 separate the individual integrated circuitry 102. Generally, the dicing streets 104 run perpendicularly to separate the integrated circuitry 102 into rows and columns. At least one guard ring 106 isolates

integrated circuitry 102 from dicing streets 104. Within the dicing streets 104, there are typically test structures that are composed of the same materials as the other parts of the interconnect layer 108. Between these test structures in the dicing street 104 and the guard ring 106 may be a region or regions composed entirely of dielectric material with no conductive material. In the embodiments that comprise two trenches, these trenches may be placed such that they fall entirely within the regions composed entirely of dielectric material. See Appellants' specification, page 6, line 18 through page 7, line 6.

Appellants' embodiment includes using a laser to ablate away two trenches (first trench 118 and second trench 118') on each of the dicing streets 104 (both row and column). The first trench 118 and the second trench 118' are positioned to reside on either side of the dicing street 104 where a saw will cut when dicing the microelectronic device wafer 100 as shown in FIGS. 2 and 3. The first trench 118 and the second trench 118' preferably extend completely through the interconnect layer 108. See Appellants' specification, page 7, lines 7-16.

In another embodiment shown in Figs. 4 and 5, an etching technique is used to form the first trench 118 and the second trench 118'. First, a resist material 122 is applied and patterned on the interconnect layer 108 such that openings 124 are created in areas where a trench is desired as shown in FIG. 4. As the entire thickness of the interconnect layer 108 is preferably removed, a relatively thick resist layer will need to be applied unless the etching selectivity is very high. As shown in FIG. 5, the interconnect layer 108 is then etched to form the first trench 118 and the second trench 118' through the semiconductor wafer 114. See Appellants' specification, page 8, lines 8-19.

After the formation of the first trench 118 and the second trench 118' and, if an etching process is used, after the removal of the resist material, a wafer saw 117 (see Fig. 6) cuts a channel 126 between the first trench 118 and the second trench 118', through the interconnect layer 108, and through the semiconductor wafer 114 as shown in Figs. 7 and 8. See Appellants' specification, page 9, lines 12-16.

Figs. 9-14 illustrate another embodiment of Appellants' invention. Instead of forming two individual

trenches as shown in Figs. 2-8, a single, wide trench 128 is formed. The wide trench 128 should be wide enough to eliminate any interaction of a wafer saw and the interconnect layer 108 during the dicing of the microelectronic device wafer. The elimination of any interaction between the wafer saw and the interconnect layer 108 eliminates the potential of any defect being generated in the interconnect layer 108 by the wafer saw. See Appellants' specification, page 9, line 18 through page 10, line 2. The single wide trench 128 may be formed by a laser as shown in Figs. 9 and 10, by etching as shown in Figs. 11 and 12, or by any method of forming such a trench known in the art. After the formation of the wide trench 128 and, if an etching process is used, after the removal of the resist material 122, a wafer saw is placed within the wide trench 128 and it cuts a channel 134 through the semiconductor wafer 114 as shown in Figs. 13 and 14. See Appellants' specification, page 10, lines 3-9.

Claim 1 is representative of the claimed invention and is reproduced as follows:

1. A method of dicing a microelectronic device wafer, comprising:

providing a microelectronic device wafer comprising a semiconductor wafer having an interconnect layer disposed thereon, said microelectronic device including at least two integrated circuits formed therein separated by at least one dicing street;

forming at least one trench through said interconnect layer within said at least one dicing street;

cutting through said semiconductor wafer within said at least one dicing street.

REFERENCES

The references relied on by the Examiner are as follows:

Mori	5,024,970	Jun. 18, 1991
Igarashi et al. (Igarashi)	6,306,731	Oct. 23, 2001 (filed Apr. 3, 2000)
Ibnabdeljalil et al. (Ibnabdeljalil)	6,365,958	Apr. 2, 2002 (filed Jan. 21, 1999)
Kroeninger et al. (Kroeninger)	DE 198 40 508 A1	Dec. 2, 1999

Stanley Wolf "Silicon Processing for the VSLI Era" Volume 1, Lattice Press 1986, Chapter 16.

REJECTIONS AT ISSUE

Claims 1, 3, 5-9, 11, 13, and 14 stand rejected under 35 U.S.C. § 103 as being obvious over Ibnabdeljalil in view of Mori. Claims 2 and 10 stand rejected under 35 U.S.C. § 103 as being obvious over Ibnabdeljalil in view of Mori and further in view of Kroeninger. Claims 4 and 12 stand rejected under

35 U.S.C. § 103 as being obvious over Ibnabdeljalil in view of Mori and further in view of Wolf.

Claims 15, 19[1], and 20 stand rejected under 35 U.S.C. § 103 as being obvious over Ibnabdeljalil in view of Igarashi. Claim 16 stands rejected under 35 U.S.C. § 103 as being obvious over Ibnabdeljalil in view of Igarashi and further in view of Kroeninger. Claim 17 stands rejected under 35 U.S.C. § 103 as being obvious over Ibnabdeljalil in view of Igarashi and further in view of Mori. Claim 18 stands rejected under 35 U.S.C. § 103 as being obvious over Ibnabdeljalil, Igarashi, Mori, and further in view of Wolf.

OPINION

With full consideration being given to the subject matter on appeal, Examiner's rejections and the arguments of Appellants and Examiner, for the reasons stated ***infra***, we reverse the Examiner's rejection of claims 1-20 under 35 U.S.C. § 103.

In rejecting claims under 35 U.S.C. § 103, the Examiner

[1] We note that claim 19 is dependent upon claims 17 and 15. Claim 19 should have been rejected or grouped with claim 17. However, the Examiner addressed claim 19 in the rejection of claims 15 and 20 as seen on page 6 of the answer. Therefore, we will group claim 19 with claims 15 and 20.

bears the initial burden of establishing a ***prima facie*** case of obviousness. ***In re Oetiker***, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). See also ***In re Piasecki***, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984). The Examiner can satisfy this burden by showing that some objective teaching in the prior art or knowledge generally available to one of ordinary skill in the art suggests the claimed subject matter. ***In re Fine***, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). Only if this initial burden is met, does the burden of coming forward with evidence or argument shift to Appellants. ***Oetiker***, 977 F.2d at 1445, 24 USPQ2d at 1444. See also ***Piasecki***, 745 F.2d at 1472, 223 USPQ at 788.

An obviousness analysis commences with a review and consideration of all pertinent evidence and arguments. "In reviewing the [E]xaminer's decision on appeal, the Board must necessarily weigh all of the evidence and argument." ***In re Oetiker***, 977 F.2d at 1445, 24 USPQ2d at 1444. "[T]he Board must not only assure that the requisite findings are made, based on evidence of record, but must also explain the reasoning by which the findings are deemed to support the agency's conclusion." ***In re Lee***, 277 F.3d 1338, 1344, 61 USPQ2d 1430, 1434 (Fed. Cir.

2002).

Rejection of Claims 1, 3, 5-9, 11, 13, and 14

First, we will address the rejection of independent claims 1 and 9 and their dependent claims 3, 5-8, 11, 13, and 14 under 35 U.S.C. § 103. Appellants argue that Ibnabdeljalil does not teach forming at least one trench through the interconnect layer within the at least one dicing street because Ibnabdeljalil merely teaches a standard technique of dicing completely through the interconnect layer and the semiconductor wafer with a dicing saw. See page 11 of the brief. The Examiner agrees with Appellants that Ibnabdeljalil fails to teach forming at least one trench through the interconnect layer. See last paragraph on page 4 of the answer. The Examiner relies on Mori for a teaching of forming a trench through the interconnect layer. See page 5 of the answer. The Appellants argue that "[a]lthough the Mori patent teaches forming a trench, it does not teach or suggest forming a trench in an interconnect layer as required by the present claims." See page 12 of the brief. More importantly, Appellants argue that Appellants' specification has defined the term

"interconnect layer" different from the ordinary meaning.

Appellants emphasize on page 12 of the brief:

The present specification states, in total, at page 6, line 10-15:

> The **interconnect layer** 108 is **generally alternating layers** 112 **of dielectric material**, including but not limited to silicon dioxide, silicon nitride, epoxy resin, polyimide, bisbenzocyclobutene, fluorinated silicon dioxide, carbon-doped silicon dioxide, silicon carbide, various polymeric dielectric materials (such as SiLK available for Dow Chemical, Midland, MI), and the like, **and patterned electrically conductive material**, including copper, aluminum, silver, titanium, alloys thereof, and the like. (Emphasis added)

Clearly, the Appellants have defined an interconnect layer as alternating layers of dielectric material and patterned electrically conductive material.

We agree that Appellants are entitled to be their own lexicographer. Our reviewing Court has stated that the presumption in favor of a dictionary definition will be overcome where the patentee, acting as his or her own lexicographer, has clearly set forth an explicit definition of the term different from its ordinary meaning. ***Texas Digital Systems, Inc. v.***

Telegenix, Inc., 308 F.3d 1193, 1204, 64 USPQ2d 1812, 1819 (Fed. Cir. 2002).

Upon our review of Appellants' specification, we find that Appellants have met the burden to overcome the presumption of customary and ordinary meaning of the term "an interconnect layer." Therefore, in determining the scope of Appellants' claims, we will adopt Appellants' specialized definition of the term "an interconnect layer" as "alternating layers of dielectric material and patterned electrically conductive material."

We note that all of the independent claims 1, 9, and 15 require forming at least one trench through an interconnect layer. Therefore, the question before us is whether Mori teaches this limitation as specifically defined. The Examiner points out that Mori's Fig. 6A teaches at least one trench in layers of silicon nitride and silicon oxide. See page 5 of the answer. We find that Mori's Fig. 6B shows the trench 14,

however, the trench 14 is in layer of silicon substrate 1. Thus, the trench 14 is not in the interconnect layer as specifically defined. Similarly, Fig. 1K of Mori shows a trench 14 through layers 4e and 1. However, Mori's layers 4e and 1 are formed of silicon oxide and silicon substrate, *i.e.*, dielectric materials only. See Mori, column 3, lines 36-37, and column 3, line 66 to column 4, line 5. Therefore, Mori's layers 4e and 1 are not formed as alternating layers of dielectric material and patterned electrically conductive material. Therefore, we find that the combination of Ibnabdeljalil and Mori does not teach or suggest forming at least one trench through an interconnect layer as required by Appellants' independent claims 1, 9 and 15.

As noted above, our reviewing court requires the requisite findings based upon the evidence of record. It is the Examiner's burden of showing the objective teachings in the prior art. We note that the Examiner has not met the burden of coming forward with the evidence of establishing a ***prima facie*** case of obviousness as set forth above. Therefore, we have not sustained the Examiner's rejection of claims 1, 3, 5-9, 11, 13, and 14 under 35 U.S.C. § 103.

Rejection of Claims 2 and 10

Dependent claims 2 and 10 are rejected under 35 U.S.C. § 103 as being obvious over Ibnabdeljalil in view of Mori and further in view of Kroeninger. We find that Kroeninger teaches the use of laser cutting to form trenches as Examiner pointed out on page 7 of the answer. However, Kroeninger does not teach the forming at least one trench through an interconnect layer as Appellants defined. Therefore, we will not sustain the rejection of claims 2 and 10.

Rejection of Claims 4 and 12

Dependent claims 4 and 12 are rejected under 35 U.S.C. § 103 as being obvious over Ibnabdeljalil in view of Mori and further in view of Wolf. We find that Wolf teaches plasma etching to form trenches as Examiner pointed out on page 8 of the answer. However, Wolf does not teach the forming at least one trench through an interconnect layer as Appellants defined. Therefore, we will not sustain the rejection of these claims 4 and 12.

Rejection of Claims 15, 19, and 20

We now address the rejection of independent claim 15 and its dependent claims 19 and 20 under 35 U.S.C. § 103 as being obvious over Ibnabdeljalil and Igarashi. We note that both Appellants and Examiner admit that Ibnabdeljalil teaches forming the interconnect layer within the at least one dicing street, but Ibnabdeljalil does not teach the trench. See last paragraph on page 14 of the brief through line 6 on page 15 of the brief, and page 6 of the answer. The Examiner relies on Igarashi for the teaching of forming at least one wide trench 103 in Fig. 12A. See page 6 of the answer. Appellants argue that "although Igarashi teaches forming a trench, Igarashi does not teach or suggest forming a trench in an interconnect layer *as required by the present claims*." (Emphasis added). See page 15 of the brief.

We find that Igarashi's Fig. 12A shows that Igarashi's wide trench 103 is formed through the layer 104. However, Igarashi's layer 104 is a conductive layer only. Thus, Igarashi does not teach the interconnect layer *specifically defined* as alternating layers of dielectric material and patterned electrically conductive material in claim 15. Consequently, we find that the

Examiner has not established a ***prima facie*** case of obviousness since the combination suggested by the Examiner does not teach or suggest "forming at least one wide trench through said microelectronic device wafer interconnect layer within said at least one dicing street" *as required* in independent claim 15. Therefore, we have not sustained the Examiner's rejection of claims 15, 19, and 20.

Rejection of Claim 16

Dependent claim 16 is rejected under 35 U.S.C. § 103 as being obvious over Ibnabdeljalil in view of Igarashi and further in view of Kroeninger. We find that Kroeninger teaches laser cutting to form trenches as Examiner pointed out on page 8 of the answer. However, Kroeninger does not teach forming at least one trench through an interconnect layer. Consequently, the combination of Ibnabdeljalil, Mori, and Kroeninger does not teach or suggest "forming at least one wide trench through said microelectronic device wafer interconnect layer within said at least one dicing street" required in claim 16. Therefore, we will not sustain the rejection of claim 16.

Rejection of Claim 17

Dependent claim 17 is rejected under 35 U.S.C. § 103 as being obvious over Ibnabdeljalil in view of Igarashi and further in view of Mori. As set forth above, we find that Mori does not teach the forming of at least one trench through an interconnect layer. Consequently, the combination of Ibnabdeljalil, Igarashi, and Mori does not teach or suggest "forming at least one wide trench through said microelectronic device wafer interconnect layer within said at least one dicing street" required in claim 17. Therefore, we will not sustain the rejection of claim 17.

Rejection of Claim 18

Dependent claim 18 is rejected under 35 U.S.C. § 103 as being obvious over Ibnabdeljalil in view of Igarashi and Mori and further in view of Wolf. We find that Wolf teaches plasma etching to form trenches as Examiner pointed out on page 8 of the answer. However, Wolf does not teach forming at least one trench through an interconnect layer. Consequently, the combination of Ibnabdeljalil, Igarashi, Mori, and Wolf does not teach or suggest the step of "forming at least one wide trench through said microelectronic device wafer interconnect layer within said at

least one dicing street" required in claim 18. Therefore, we will not sustain the rejection of claim 18.

In view of the foregoing, we have not sustained the Examiner's rejection of claims 1-20 under 35 U.S.C. § 103.

REVERSED

MICHAEL R. FLEMING Administrative Patent Judge	)	
JOSEPH F. RUGGIERO Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
HOWARD B. BLANKENSHIP Administrative Patent Judge	)	

MRF: lbg

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